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Abstract

Focal plane arrays (FPAs) are used in many applications for detecting infrared (IR) radiation where normal sight with light in the visible spectrum is not possible. To effectively detect this IR radiation, complex semiconductor diodes, cooled to low temperatures, are usually used. The most common of these semiconductor materials is the II-VI alloy semiconductor system using HgCdTe, which is often called MCT. Focal plane arrays with over 1000 pixels have been fabricated. The cost of these very complex systems is becoming a very important consideration in decisions of where to use these FPAs.

The focal plane array actually consists of two semiconductor parts with a sophisticated cooling assembly. The semiconductor parts are the MCT detector device itself and a companion device called the read-out circuit. The cost model presented in this paper consists of various expressions as functions of physical parameters that can be measured, calculated from data or estimated. Although accurate absolute cost data may not be available (because it does not exist or is proprietary to a company), cost estimates can be effectively used to determine relative cost between two designs or processes. In addition, when these cost models are coupled with the STADIUM design of experiments simulation methodology, accurate predictions of the most dominant cost drivers can be obtained. This cost model and its algorithms are coupled with a commercial software program called IR-SIM.

KEY WORDS: FPA Cost, FPA design, modeling, system design, optimized performance, STADIUM

1. INTRODUCTION

The focal plane array (FPA) detector is used in many military applications where normal sight with light in the visible spectrum is not possible. These conditions include not only night vision but also a variety of adverse atmospheric conditions such as smoke and fog. In these conditions, objects are detected not by the visible light they give off but by the infrared (IR) energy they radiate. To effectively detect this IR radiation, complex semiconductor diodes cooled to low temperatures are usually used. The most common of these materials is the II-VI alloy semiconductor HgCdTe, which is often called MCT.

Compound Semiconductor devices have been used for many years for the detection of infrared radiation but few adequate computer models exist. FPA detectors are semiconductor devices that detect long wave photons (1 to 20 microns) by interaction of the radiation with the atomic lattice of the material creating hole-electron pairs. The 1 micron wavelength region of the radiation spectrum is called the Short Wavelength Infrared (SWIR) region while the 20 microns region is called the Very Long Wavelength Infrared (VLWIR) region. Thus, 1 to 20 microns is referred to as the SWIR-VLWIR region. We have developed a robust simulation methodology to predict the results of these devices [1,2].

The focal plane array detector actually consists of two parts assembled together. These are the MCT detector device itself and a companion device called the read-out circuit. The read-out circuit is usually an array of amplifiers on a silicon chip. This chip uses common integrated circuit processing and is physically and electrical connected to the MCT detector device.

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The cost equations presented below are expressed as functions of physical parameters that can either be measured, calculated from data or estimated. Although accurate absolute cost data may not be available (because it does not exist or is proprietary to a company), cost estimates can be effectively used to determine relative cost between two designs or processes. In addition, when these cost models are coupled with the STADIUM design of experiments simulation methodology [3], accurate predictions of the most dominant cost drivers can be obtained.

The cost of the completed FPA detector device can be expressed as the sum of the cost of the MCT detector chip, the cost of the read-out circuit and the cost to assemble them together into a single unit. This total detector cost can be expressed as shown in equation 1.

$$C_t = C_d + C_r + C_a \tag{1}$$

Where,
C_t = Total Detector Cost
C_d = Cost of MCT Detector Chip
C_r = Cost of Read-out Circuit per chip
C_a = Assembly Cost.

The goal of the cost analysis will then be to calculate the cost of the pieces and add the costs together. In most cases, the cost of the MCT chip will dominate the total, and therefore we will pay more attention C_d in the analysis. The cost per pixel (C_p) is given by:

$$C_p = C_t / N_p \tag{1a}$$

Where,
N_p = Number of diodes or pixels per chip.

2. DETECTOR CHIP COST

The cost of the detector chip is considered to be the sum of the material cost and the diode fabrication cost. To obtain the cost for each detector we divide the total wafer cost by the number of good detectors obtained per wafer, as shown in equation 2.

$$C_d = [C_{m/w} + C_{f/w}] / N_{dg} \tag{2}$$

Where,
$C_{m/w}$ = Material Cost per wafer
$C_{f/w}$ = Fabrication Cost per wafer
N_{dg} = Number of Good detector die per wafer.

The number of good detector die is a product of the average yield of detector chips on the wafer times the total number of possible detector chips on each wafer. This is expressed in equation (3). Note the N_{dg} must be rounded down to the nearest integer.

$$N_{dg} = [A_{dw} / A_d] * P_{wd} * Y_{dp} \tag{3}$$

Where,
P_{wd} = Percent of wafer that is usable for detectors
A_{dw} = Area of the starting detector wafer
A_d = Area of the detector chip
Y_{dp} = Yield of good detectors per wafer.

The area of the detector chip is a function of the number of diodes or pixels on the detector as well as the area required on the periphery of the chip for any bond wires or regions of test structures. This can be calculated by using equation 4 with the details shown in Figure 1.

$$A_d = A_p * N_p + 4 * L_p * [L_p + \sqrt{(A_p * N_p)}] \quad (4)$$

And

$$A_p = L_d^2 \quad (4a)$$

Where,
A_p = Chip area of each pixel
N_p = Number of diodes or pixels per chip
L_p = Length of chip periphery region of the chip
L_d = distance between center points of adjacent pixels.

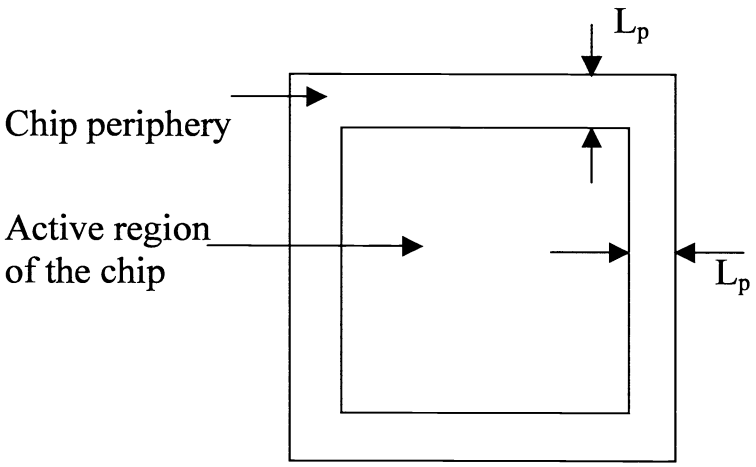

Figure 1. The geometry of the detector chip.

The yield of the detector chip represents the number of good detectors obtained versus the total number of possible chips produced. It is an inverse function of the area of the detector chip and the density of destructive defects on the MCT wafer. Much research with silicon integrated circuits has shown that the yield for actual distributed defects can by estimated using equation 5.

$$Y_{dp} = 1/[A_d * D_d + 1] \quad (5)$$

Where,
D_d = Defect density of detector chip.

The defect density can be calculated as the sum of defects created during the material preparation and defects created during the processing of the detector diodes. The latter can be proportional to the number of critical fabrication steps required for a specific detector configuration. This defect density is obtained through equation 6.

$$D_d = D_m + D_p * N_f \quad (6)$$

Where,
D_m = Material defect density
D_p = Fabrication step defect density
N_f = Number of critical fabrication steps.

3. READ-OUT CIRCUIT CHIP COST

The silicon read-out chip is usually produced by a commercial integrated circuit fabrication facility and is sold to the focal plane array producer in either wafer or chip form. The cost per read-out chip is then given by the cost of the wafer divided by the number of good read-out circuits obtained per wafer. This is given by equation 7.

$$C_r = C_{r/w} / N_{rg} \tag{7}$$

Where,
$C_{r/w}$ = Cost per wafer
N_{rg} = Number of Good Read-out die per wafer

The number of good read-out circuits per wafer is the ratio of the areas of the wafer and the read-out chip times the yield if the circuits. Equation 8 can be used to calculate this.

$$N_{rg} = [A_{rw} / A_r] * P_{wr} * Y_{rp} \tag{8}$$

Where,
P_{wr} = Percent of wafer that is usable for read-outs
A_{rw}= Area of the starting read-out wafer
A_r = Area of the read-out chip
Y_{rp} = Yield of good read-outs per wafer

In some cases, the area of the read-out circuit is designed to be the same as the area of the detector chip so that a "bump" assemble process can be used to put them together. The yield of the read-out circuits can be calculated in a manner similar to the yield of the detector chips. Equation 9 can be used in this case.

$$Y_{rp} = 1/ [A_r * D_r + 1] \tag{9}$$

Where,
D_r = Total defect density for the read-out circuit.

4. ASSEMBLY COST

The cost to physically and electrical attach the detector chip and the read-out circuit plus packaging of the entire device is called the Assembly Cost. This will be a function of the number of diodes (pixels) because there must be at least one bond between the detector chip and the read-out circuit per diode. The cost shown below in equation 10 does not include the cost of a dewar or other cooling equipment and other electrical and mechanical parts of the system.

$$C_a = C_p + C_b * N_p \tag{10}$$

Where,
C_a = Assembly Cost
C_p = Packaging Cost
C_b = Cost per bond
N_p = Number of diodes or pixels per detector chip.

The following sections begin with a discussion of modeling methodologies used in this project. AET has used MCT device physics analysis in modeling the performance of double layer heterojunction MCT devices. Traditional semiconductor device physics are coupled with a variety of material models to accurately simulate the electrical characteristics of devices. AET used this approach as a basis in developing an overall model. Actual heterojunction FPA devices have been fabricated and tested for cross talk, and this data is compared to the simulation results.

5. EXAMPLE COST ANALYSIS

AET, Inc. has incorporated this model into a commercial software tool. For government managers and systems designers, accurate cost driver information may not be available. Therefore, this tool can be used to develop economic comparisons between technologies as shown in the table below. For engineers who manufacture the MCT devices and focal plane arrays, proprietary cost information will be entered into the model and thus accurate cost predictions will be obtained.

Presented in the table below are the results of using this cost model to calculate comparative costs between different MCT technologies and different FPA sizes. The cost and technology data presented in this table is primarily the "best guess" of the AET engineers based on discussions with industry scientists and information obtained from the IRIS meetings. Actual data is very difficult to obtain because most manufacturers feel that this is some of their most proprietary information.

The two FPA sizes considered are the 64X64 array (4096 pixels) and the 256X256 array (65536 pixels). The primary effect of the larger number of pixels is to increase total chip area required and decrease yields. These both greatly increase FPA costs but as shown in the table, the cost per pixel decreases significantly as the number of pixels increases.

The two technologies considered are the older liquid phase epitaxy (LPE) process and the newer molecular beam epitaxy (MBE). The LPE technology uses a mesa etch process to define the individual MCT diodes and with a diode to diode center line spacing of 40 microns. The MBE technology uses photolithography and ion implantation processes to define each diode. This allows diodes to be placed much closer together with a diode to diode center line spacing of 20 microns. These spacing assumptions discussed above have not been obtained from any actual data, but were devised to illustrate the the utility of the model.

Results of this sample cost analysis is shown in Table 1. The bottom line results show that the cost per pixel of the 64X64 FPA is lower for the LPE technology versus the MBE technology. This is because the processing cost of the MBE dominates the cost.

The cost per pixel of the 256X256 FPA is higher for the LPE technology versus the MBE technology. This is because the packaging and assembly cost dominates for the very large arrays.

Table 1. Example Values for Variables of Specific MCT Technologies

Variables	LPE Mesa 64x64	LPE Mesa 256x256	MBE I^2 64x64	MBE I^2 256x256
Independent				
$C_{m/w}$ ($/wafer)	1000	1000	2000	2000
$C_{f/w}$ ($/wafer)	2000	2000	8000	8000
P_{wd} (no units)	1	1	1	1
A_{dw} (cm^2)	6	6	6	6
L_d (cm)	0.004	0.004	0.002	0.002
A_p (cm^2)	0.000016	0.000016	0.000004	0.000004
N_p (no units)	4096	65536	4096	65536
L_p (cm)	0.1	0.1	0.1	0.1
D_m(defects/cm^2)	0.5	0.5	0.5	0.5
D_p (defects/cm^2)	0.2	0.2	0.1	0.1
N_f (no units)	4	4	5	5
$C_{r/w}$ ($/wafer)	2000	2000	2000	2000
P_{wr} (no units)	0.8	0.8	0.8	0.8
A_{rw} (cm^2)	78.5	78.5	78.5	78.5
D_r (defects/cm^2)	2	2	2	2
C_p ($/wafer)	500	1000	500	1000
C_b ($/wafer)	0.01	0.01	0.01	0.01
Dependent				
A_d (cm^2)	0.21	1.50	0.11	0.51
Y_{dp} (no units)	0.79	0.34	0.90	0.66
N_{dg} (no units)	22.71	1.36	50.35	7.85
D_d(defects/cm^2)	1.30	1.30	1.00	1.00
C_d ($/chip)	132.07	2208.03	198.60	1273.23
N_{rg} (no units)	213.31	10.49	480.37	61.51
A_r (cm^2)	0.21	1.50	0.11	0.51
Y_{rp} (no units)	0.71	0.25	0.82	0.50
C_r ($/chip)	9.38	190.68	4.16	32.51
C_a ($)	540.96	1655.36	540.96	1655.36
C_t ($/unit)	682.41	4054.07	743.72	2961.10
C_p ($) Cost/pixel	0.167	0.062	0.182	0.045

6. COST MODEL USER INTERFACES

Figure 2 shows the user interface for the MCT cost model. All inputs to the model are entered through this interface. All data entered may also be saved and re-loaded for subsequent analysis.

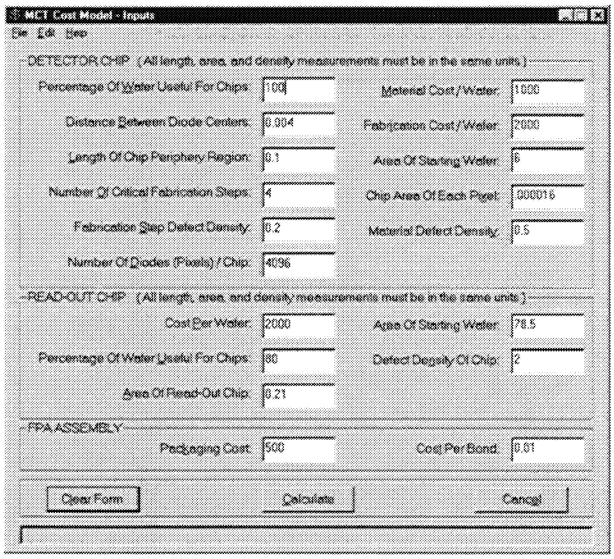

Figure 2. Input Interface for the Cost Model

By clicking on the "Calculate" button, the MCT cost model calculates a number of cost parameters associated with the FPA. These parameters are displayed in the output user interface shown in Figure 3.

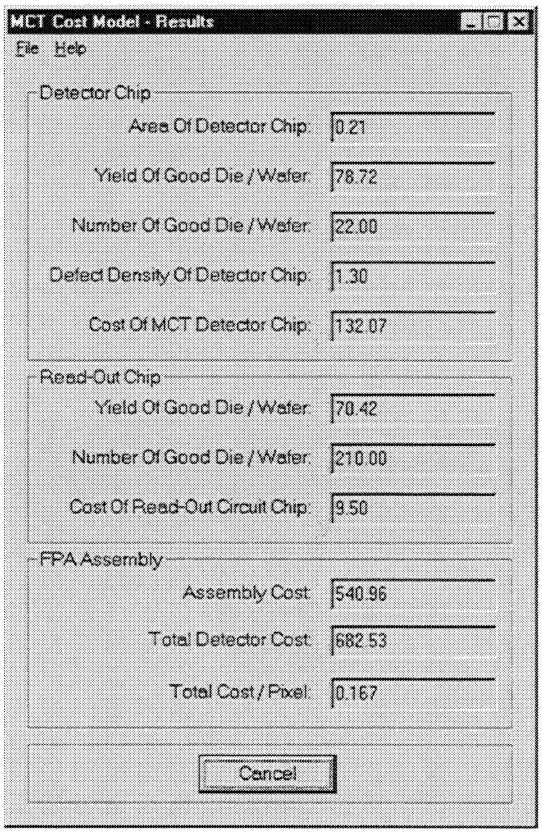

Figure 3. Output Interface for the Cost Model

7. CONCLUSIONS

This paper has described the new heterojunction MCT model methodology developed by AET, Inc. and Florida Institute of Technology for the US Army under an SBIR contract. This methodology uses basic physics to model this complex device. Initial results of the comparison of the simulation output with experimental data is very encouraging. The new MCT cross talk model is being used in conjunction with the AET IRSIM software to allow the engineer to accurately predict the photocurrent response for the focal plane array.

To improve the manufacturability and cost metrics associated with the focal plane array, AET has employed advanced statistical techniques to improve the FPA detector model developed in this program. Specifically, we utilize the statistical technique known as design of experiments (DoE). This technique is embodied in a software technology called STADIUM, which has been developed by Florida Institute of Technology under funding from SEMATECH. The use of STADIUM leads to a comprehensive understanding of the relationship between the input parameters and the output of the detector. This is called "design for manufacturing." In addition, the statistical design of experiments methodology leads to fabrication process optimization through the use of Taguchi techniques.

8. ACKNOWLEDGMENTS

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